

Jae-Yun Park

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EDUCATION

- 2022 – Present Master of Science Candidate in Department of Electronic Engineering
Seoul National University of Science and Technology (SeoulTech), Seoul, South Korea
- 2015 – 2021 Bachelor of Science in Electronic Engineering
SeoulTech, Seoul, South Korea

RESEARCH EXPERIENCES

Research Assistant, Dept of Electronic Engineering, SeoulTech.

Advisor: Jae-Won Nam (2022 ~ Present).

- Cell based full-custom AMS circuit design.
- Delta-Sigma DAC for Quantum computing systems.
- SRAM-based PUF (Physical Unclonable Function) circuits and systems.

Tape-out

- 2023.11. Samsung 28nm Bulk CMOS, ADPLL.
- 2023.11. Samsung 28nm FD-SOI, SRAM based PUF circuits and Incremental-ADC.
- 2023.09. TSMC 65nm LP, 4-channel TI Delta-Sigma DAC.
- 2023.07. Samsung 28nm Bulk CMOS, ADC (Domino SAR, Flash) and temperature sensor.
- 2023.05. TSMC 180nm BCD, SRAM based PUF circuits.
- 2023.05. NNFC 180nm Bulk CMOS, CMOS Image Sensor (CIS) ROIC.
- 2023.02. Samsung 28nm Bulk CMOS, SRAM based PUF circuits.

RESEARCH PROJECTS

- Monolithic Colloidal Quantum Dot-based Image Sensor (2023.07. ~ 2025.11.).
 - ✓ Role: Student researcher
 - ✓ Subjects: Silicon ROIC / Column Decoder.
- Scalable and Reliable Cryogenic CMOS Interconnect Electronics (2021.09. ~ 2024.02.).
 - ✓ Role: Student researcher
 - ✓ Subjects: Cryogenic CMOS Data converter / 4-channel TI Delta-Sigma DAC.
- Hardware-based Lightweight Authentication Security System-on-Chip (SoC) using Physically Unclonable Circuits. (2021.09. ~ 2024.02.)
 - ✓ Role: Student researcher

- ✓ Subjects: SRAM-based PUF circuits / SRAM CRP Post-processing.
- Next-Generation Semiconductor Design Workforce Development Program (2021.03. ~ 2026.02.).
- ✓ Role: Student researcher
- ✓ Subjects: Sigma-Delta Modulator / Decimation Filter.

LIST OF PUBLICATIONS

Journal

- **J.-Y. Park** and J.-W. Nam, “A 4.3 GS/s time-interleaved $\Delta\Sigma$ DAC with temperature-insensitive bias and harmonic cancellation for qubit control,” *IEEE Trans. Circuits Syst. II: Express-Briefs*, vol. 71, no. 11, pp. 4663-4667, Sep. 2024.
- K. Yu, J. Yoo, H. Yoo, **J.-Y. Park**, H. J. Yook, J. H. Cho, Y. K. Lee, J.-P. Hong, and J.-W. Nam, “Adjustable majority voting algorithm for stability improvement in sRAM-based CMOS PUFs,” *IEEE Trans. VLSI*, vol. xx, no. xx, pp. xx-xx, Nov. 2024. (**Submitted**)
- **J.-Y. Park**, S.-H. Kim, H. Yoo and J.-W. Nam, “Analysis of quarter method applied ROM-based DDFS architecture,” *IEEE Access*, vol. 11, pp. 117137-117148, Oct. 2023.

Conference

- **J.-Y. Park** and J.-W. Nam, “4 GS/s 4-way time-interleaved noise-shaped DAC for qubit control using quarter method DDFS,” *Winter annual conference of KIEES*, Jeju, Feb. 2024.
- **J.-Y. Park**, S.-H. Kim, and J.-W. Nam, “Analysis of ROM-based DDFS architecture employing quarter method,” in *Proc. IEEE International Conference on Electronics, Information, and Communication (ICEIC) Singapore*, Feb. 2023, pp. 788-790.
- **J. -Y. Park**, S. -H. Kim, S. G. Kim, J. -W. Hyun, Y. -S. Kim, and J. -W. Nam, “Study on direct digital frequency synthesis,” *22nd RF/Analog Circuit Workshop*, Jeju, Sep. 2022.

Chip Design Contest

- **J.-Y. Park**, D. Kim, J.-W. Hyun, J. Yoo, K. Yu, and J.-W. Nam, “A 4.3 GS/s Time-Interleaved $\Delta\Sigma$ DAC with Harmonic Cancellation for Qubit Control,” in *Proc. 21st International SoC Design Conference (ISOC2024)*, Sapporo, Japan, Aug. 2024. (**Submitted**)

TEACHING EXPERIENCE

- **Teaching Assistant**, Dept. of Electronic Engineering, SeoulTech.

- Electronic Circuit 2, Fall 2023.
- Integrated Circuit, Spring 2023.
- Electronic Circuit, Fall 2022 and Spring 2023.

Training Activities

- 2023.05.15-05.19, [IDEC Researcher Education] Cell-Based Chip Design Flow Education
- 2022.12.05-12.06, [IDEC Education] Low Noise OPAMP Design