

Jin-Won Hyun

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EDUCATION

- 2023 – Present Master of Science Candidate in Electronic Engineering
Seoul National University of Science and Technology, Seoul, South Korea
- 2017 – 2023 Bachelor of Science in Electronic and IT Media Engineering
Seoul National University of Science and Technology, Seoul, South Korea

RESEARCH EXPERIENCES

Research Assistant, Dept. of Electronic Engineering, Seoul National University of Science and Technology. Advisor: Jae-Won Nam (2022 ~ Present)

- Clock generation circuits (DLL/PLL) for high-speed interface circuit
- AMS and EM circuit design automation (SPICE / EM simulator)
- Schematic & Layout Migration Skills (Cadence)
- DAC Core & Top Bias Design for Qubit controller interface circuit
- Timing generator for CIS ROIC
- Programming Language : C, Matlab, Python, SKILL, Verilog HDL
- EDA Tools : Cadence Virtuoso/EMX, Mentor Calibre, Ngspice, Synopsys VCS/DC/FM/STA/ICC2, Ansys HFSS

Intern, Point2Technology, RF Team intern, (2024.06 ~ 2024.12)

- EM verification and optimization ([PCB] TLine, [Package] TLine/Antenna, [Module] Deflector)

Tape-out

- 2024.07. Samsung 28nm DDFS/DSM/DAC ($4 \times 4 \text{ mm}^2$). (CLOCK BUF)
- 2024.01. Samsung 28nm ADPLL ($4 \times 4 \text{ mm}^2$). (TOP / ADPLL)
- 2023.12. NNFC 180nm Bulk CMOS, CMOS Image Sensor (CIS) ROIC ($7 \times 7 \text{ mm}^2$). (Migration)
- 2023.09. TSMC 65nm DDFS/DSM/DAC ($4 \times 4 \text{ mm}^2$). (DAC / Bias circuit / Mux)
- 2023.07. Samsung 28nm Domino ADC ($4 \times 4 \text{ mm}^2$). (TOP / OSC)
- 2023.05. TSMC 180nm BCD, SRAM PUF. (Test Pattern)
- 2023.05. NNFC 180nm Bulk CMOS, CMOS Image Sensor (CIS) ROIC ($4 \times 4 \text{ mm}^2$). (Migration / Timing Generator)

HONORS / AWARDS

- ISOCC Chip Design Contest Best Poster Awards, 2024.
- Magna cum Laude from Seoul Tech, 2023.

LIST OF PUBLICATIONS

- International Journal

- **J. -W. Hyun** and J. -W. Nam, “AMS Circuit Design Optimization Technique Based on ANN Regression Model with VAE Structure,” *IEEE ACCESS*, Jun. 2023, doi: [10.1109/ACCESS.2023.3285113](https://doi.org/10.1109/ACCESS.2023.3285113).

- International Conference

- **J. -W. Hyun**, D. Kim, K. -S. Choi, and J. -W. Nam, “AI-Assisted Design Automation of Circular and Asymmetric Inductor in CMOS Technology,” *Int. SOC Conf. (ISOCC)*, Sapporo, Aug. 2024, doi: [10.1109/ISOCC62682.2024.10762371](https://doi.org/10.1109/ISOCC62682.2024.10762371).
- **J. -W. Hyun** and J. -W. Nam, “Regression Model-based VCO Design Optimization Technique,” *Int. Conf. on Electronics Information and Communication (ICEIC)*, Singapore, Feb. 2023, doi: [10.1109/ICEIC57457.2023.10049908](https://doi.org/10.1109/ICEIC57457.2023.10049908).

- Domestic Conference

- H. Yoo, **J. -W. Hyun**, J.-W. Nam, “Bootstrap S/H design optimization using ANN,” *the 5th ISE Conf.*, Seoul, Dec. 2022.
- **J. -W. Hyun**, J. -Y. Kim, S. -J. Kim and J. -W. Nam, “Study on Jitter Analysis and Reduction Methods in DLL,” *Autumn Annual Conf. of IEIE*, Gyeongnam, Nov. 2022.
- J. -Y. Park, S. -H. Kim, S. G. Kim, **J. -W. Hyun**, Y. -S. Kim, and J. -W. Nam, “Study on Direct Digital Frequency Synthesis,” *22nd RF/Analog Circuit Workshop*, Jeju, Sep. 2022.

PATENTS

- J.-W. Nam, **J. -W. Hyun**, “Mixed-signal integrated circuit design optimization technique using genetic algorithm and machine learning,”
- J.-W. Nam, **J. -W. Hyun**, “Integrated circuit design system,”

TEACHING EXPERIENCE

- **Teaching Assistant**, Dept. of Electronic Engineering, Seoultech.
- Capstone Design, Spring 2023 and Spring 2024.
- Integrated Circuit, Spring 2023.
- Electronic Circuit, Fall 2022 and Spring 2023.

TRAINING ACTIVITIES

- 2023.05.15-05.19, [IDEC Researcher Education] Cell-Based Chip Design Flow Education
- 2023.02.12-02.17, [KIRD Education] Advanced semiconductor design (VCO)
- 2022.12.05-12.06, [IDEC Education] Low Noise OPAMP Design
- 2022.12.02-12.02, [IDEC Education] PLL design and analysis of jitter
- 2022.09.15-09.16, [Cadence] Mixed Signal Simulation Using Spectre AMS Designer-AVUM
- 2022.07.25-07.29, [IDEC Education] Physical Design automation algorithm (Basic)
- 2022.07.22-07.22, [IDEC Education] Noise analysis of analog circuits
- 2022.02.13-03.12, [Letuin] Full-Custom IC Design (FLASH ADC)
- 2022.02.10-02.11, [IDEC Education] Intuitive analysis of analog circuits